SPECIFICATION

Electronic Version 1.2.8
Stylesheet Version 1.0

[METHOD AND RELATED APPARATUS FOR DRIVING AN LCD MONITOR]

Background of Invention

[0001] 1.Field of the invention

[0002] The present invention relates to a method and a related apparatus for driving an LCD monitor, and more particularly, to a method and a related apparatus which can drive pixels located in a row of the LCD panel toward a target level so as to display a uniform gray level.

[0003] 2.Description of the prior art

[0004] The advantages of the liquid crystal display (LCD) include lighter weight, less electrical consumption, and less radiation contamination. Thus, the LCD has been widely applied to several portable information products such as notebooks, and PDAs. The LCD gradually replaces the cathode ray tube (CRT) monitors of the conventional desktop computers. The incident light will produce different polarization or refraction effects when alignment of these liquid crystal molecules is different. The LCD utilizes the characteristics of the liquid crystal molecules to generate red, blue, and green lights with different intensities of gray level to produce gorgeous images.

[0005] Please refer to Fig.1 of a schematic diagram of a conventional thin film transistor (TFT) liquid crystal display (LCD) 10. The LCD 10 comprises an LCD panel 12, a control circuit 14, a first driving circuit 16, a second driving circuit 18, a first power supply 20, and a second power supply 22. The LCD panel 12 is composed of two substrates and an LCD layer interposed between the two substrates. A plurality of data lines 24, a plurality of gate lines 26, which are perpendicular to the data lines 24, and a plurality

of thin film transistors 28 are disposed on one of the two substrates. A common electrode is disposed on the other substrate for providing a constant voltage Vcom via the first power supply 20. For easier description, only one thin film transistor 28 is illustrated in Fig. 1. However, a plurality of thin film transistors 28 are respectively disposed on intersections of the data lines 24 and the gate lines 26 in fact. Thus, the thin film transistors 28 are arranged on the LCD panel 12 in a matrix format. In another words, each of the data lines 24 corresponds to one column of the TFT LCD 10, each of the gate lines 26 corresponds to one row of the TFT LCD 10, and each of the thin film transistors 28 corresponds to one pixel. In addition, the two substrates of the LCD panel 12 can be regarded as an equivalent capacitor 30 according to their electrical performance.

[0006]

The driving method of the conventional TFT LCD 10 is described as follows. The control circuit 14 is used to control driving process of the TFT LCD 10. When the control circuit 14 receives horizontal synchronization 32 and vertical synchronization 34, the control circuit 14 inputs corresponding control signals to the first driving circuit 16 and the second driving circuit 18 respectively. Then, the first driving circuit 16 and the second driving circuit 18 generate input signals for each data line 24, for instance DL3, and each gate line 26, for instance GL3, according to the control signals so as to control conductance of the thin film transistors 28 and voltage differences between two ends of the equivalent capacitors 30 and to rearrange the alignment of the liquid crystal molecules and the corresponding light transmittance in advance. For example, the second driving circuit 18 inputs a pulse to the gate lines 26 so as to make the thin film transistors 28 conduct. Thus, the signals from the first driving circuit 16 to the data lines 24 can be input to the equivalent capacitors 30 via the thin film transistors 28 so as to control the gray levels of the corresponding pixels. In addition, different signals input to the data lines 24 from the first driving circuit 16 are generated based on the voltages V_0 ~V"m transmitted by the second power supply 22. The first driving circuit 16 has a voltage divider 17 for generating a plurality of voltages V_0 , ... ,Vn based on the voltages V_0 ,...,V"m. For example, the second power supply 22 is capable of outputting 10 different voltages V_0 , ... ,V"$_9$. Therefore, the voltage divider 17 is capable of dividing each of the 10 different voltages V_0 , ... ,V_9 to generate 256 different voltages V_0 ~V_{255} . Then, the first

driving circuit 16 drives the thin film transistors 28 by selecting one adequate voltage out of the voltage V_0, ... ,V_{255} according to the display data 36. Generally speaking, different voltages correspond to different gray levels. A display related to the display data 36 will be shown on the LCD panel 12 in the end.

[0007]

Please refer to Fig.1 and Fig.2. Fig.2 is a schematic diagram of the first driving circuit 16 shown in Fig.1. The first driving circuit 16 further comprises a voltage selection module 56 and an operational amplifier circuit 37 for driving the corresponding thin film transistors 28 respectively according to the different voltages V_0 to Vn generated by the voltage divider 17. The operational amplifier circuit 37 comprises a plurality of operational amplifiers 44, 45, 46, 47, 48 and 49. Each of the operational amplifiers 44, 45, 46, 47, 48 and 49 is used to form an output buffer that has a unity gain. In addition, each operational amplifier 44, 45, 46, 47, 48, 49 in the operational amplifier circuit 37 is electrically connected to a corresponding multiplexer (MUX3 to MUX8 shown in Fig.2) positioned within the voltage selection module 56. It is noteworthy that only six operational amplifiers and related multiplexers are shown in Fig.2 for simplicity. According to the control signals D3 to D8 outputted from the control circuit 14, the corresponding multiplexers will select one specific voltage level from the different voltages (V_0 to V_n) generated by the voltage divider 16. Each of the multiplexer (MUX3 to MUX8 for example) functions as an analog-to-digital decoder (DAC) to decode the corresponding display data 36. After decoding the display data 36, the multiplexer is capable of selecting one of the voltages V_0, ... ,Vn. In other words, the first driving circuit 16 is used for selecting one of the voltages V_0, ... ,Vn and outputting the selected voltage to a corresponding pixel according to the display data 36. It is noteworthy that each voltage level V_0, ... ,Vn is individually transmitted via a power transmission line such as a metal wire 66 shown in Fig.2. When the control circuit 14 receives the horizontal synchronization 32 and the vertical synchronization 34, corresponding signals are then generated and are inputted to the first driving circuit 16, and the second driving circuit 18. For example, when the second driving circuit 18 generates a pulse to make all thin film transistors located in one row conducted, that means thin film transistors 38, 39, 40, 41, 42 and 43 are conducted. The first driving circuit 16 determines that DL3, DL4, DL5, DL6, DL7, and DL8 in the data lines 24 should be driven under the

voltage V_1 according to the display data 36 so as to drive the thin film transistor 38, 39, 40, 41, 42 and 43 toward the target voltage V_1 via the operational amplifier circuit 37. Therefore, the multiplexers MUX3, MUX4, MUX5, MUX6, MUX7, and MUX8 related to the operational amplifiers 44, 45, 46, 47, 48, and 49 are controlled to select the required voltage level such as V_1. The operational amplifiers 44, 45, 46, 47, 48, and 49 take the voltage level, for instance V_1, as an input voltage to drive the thin film transistor 38, 39, 40, 41, 42, and 43 later. However, the operational amplifiers 44, 45, 46, 47, 48 and 49 have different offsets affecting the actual output voltages so that the voltage differences of the capacitors 50, 51, 52, 53, 54, and 55 are different. According to the display data 36, the pixels corresponding to DL3, DL4, DL5, DL6, DL7, and DL8 in the data lines 25 should display the same gray level. However, the gray levels in the display screen are not uniform because different offsets of the output voltages are made by the operational amplifiers 44, 45, 46, 47, 48 and 49, which therefore deteriorates the display quality.

Summary of Invention

[0008] It is therefore a primary objective of the claimed invention to provide a method for driving an LCD monitor which can make pixels located in the same row of the LCD panel have the same target level so as to display a uniform gray level.

[0009]

In a first preferred embodiment, the claimed invention provides a method of driving a liquid crystal display (LCD) monitor. The LCD monitor comprises an LCD panel for displaying a plurality of pixels arranged in a matrix format, and a voltage selection unit comprising a plurality of power transmission lines for outputting a plurality of voltages according to display data. The power transmission lines of the voltage selection unit are electrically connected to a plurality of driving units. Each driving unit comprises an output buffer and a switch. A first end of the switch is connected to either an output terminal of the output buffer or an input terminal of the output buffer. A second end of the switch is connected to an output terminal of the driving unit. The method comprises connecting the first end of the switch to the output terminal of the output buffer for driving an output voltage of the driving unit toward a voltage transmitted via the power transmission line of the voltage selection unit, and connecting the first end of the switch to the input terminal of the output

buffer for driving the output voltage of the driving unit toward an average voltage generated from averaging voltages at output terminals of the driving units that are driven through the same voltage outputted from the same power transmission line.

[0010] In a second preferred embodiment, the claimed invention provides a method of driving a liquid crystal display monitor according to a line inversion method. The LCD monitor comprises an LCD panel for displaying a plurality of pixels arranged in a matrix format, and a voltage selection circuit comprising a plurality of output terminals for outputting a plurality of voltages. Each output terminal of the voltage selection circuit is selectively and electrically coupled to a driving unit. The driving unit comprises an output buffer, a first switch electrically connected to an output terminal of the output buffer and an output terminal of the driving unit, and a second switch connected to an output terminal of two adjacent driving units. The output terminal of the output buffer is electrically connected to the output terminal of the driving unit when the first switch is turned on, and the output terminal of one driving unit is electrically connected to the output terminal of another driving unit when the second switch is turned on. The method comprises turning on the first switch for driving an output voltage of the driving unit toward a voltage of the output terminal of the voltage selection unit that is connected to the driving unit, and turning on the second switch for driving the output voltage of the driving units toward an average voltage generated from averaging voltages at output terminals of the driving units when the driving units are connected to output terminals of the voltage selection unit that provide the same voltage.

[0011] In the third embodiment, the claimed invention provides a method of driving a liquid crystal display monitor according to a column inversion method, a dot inversion method, and a two dot line inversion. The third embodiment is based on the second preferred embodiment, and the principal difference is that the second switch is connected to output terminals of two driving units with at least one another driving unit positioned between the two driving units. Therefore, the two driving units connected by the second switch are prepared to drive corresponding pixels with voltages having the same polarity and drive the pixels to the same gray level.

[0012] The claimed invention further discloses a timing controller used to control the

switches. The timing controller has a frequency divider, a counter, and a comparator for generating an output signal. A switch controller controls switches according to the output signal. In addition, an external clock generator can also be used to generate a clock signal to replace the output signal generated from the timing controller, and the switch controller uses the clock signal instead of the output signal to control switches. The operating voltages inputted into the operational amplifiers are cut off for saving power because the voltages inputted into pixels are averaged with the help of switches without being driven by the operational amplifiers anymore.

[0013] It is an advantage of the claimed invention that the pixels located in a row have the same target voltage so as to display data in a uniform gray level.

[0014] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment which is illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a schematic diagram of a conventional thin film transistor liquid crystal display monitor.

[0016] Fig.2 is a schematic diagram of the first driving circuit shown in Fig.1.

[0017] Fig.3 is a schematic diagram of a first operational amplifier circuit according to the present invention.

[0018] Fig.4 is a schematic diagram of a second operational amplifier circuit according to the present invention.

[0019] Fig.5 is a schematic diagram of a third operational amplifier circuit according to the present invention.

[0020] Fig.6 is a simplified diagram of a connection between pixels and the third operational amplifier circuit shown in fig.5.

[0021] Fig.7 is a block diagram of a timing controller according to the present invention.

[0022] Fig.8 is a timing diagram of the timing controller.

Detailed Description

[0023] Please refer to Fig.1, Fig.2, and Fig.3. Fig.3 is a schematic diagram of a first operational amplifier circuit 60 according to the present invention. The operational amplifier circuit 60 in the present invention is used to replace the operational amplifier circuit 37 located in the first driving circuit 16 shown in Fig.2. Please note that the detailed operation of the voltage selection module 56 has been described before in the prior art section, and the lengthy description is not repeated again for simplicity. The operational amplifier circuit 60 comprises a plurality of operational amplifiers 62 or operational transconductance amplifiers (OTA) to form output buffers with a unity gain and a plurality of switches 64 for controlling current routes. When the second driving circuit 18 inputs a pulse to the gate lines 26 according to the horizontal synchronization 32, all thin film transistors 28 in the same gate line 26 conduct. Thus, the first driving circuit 16 respectively outputscorresponding voltages to DL1, DL2, DL3, ... DLn in the data line 24according to the display data 36 so as to display corresponding gray levels on the LCD panel 12. At this time, the multiplexer corresponding to the operational amplifier 62 is controlled to select a required voltage such as V_1, and the switch 64 is switched to conduct two ends E1 and E2 so that the voltage V_1 can drive the capacitor 30 through the operational amplifier 62. However, each operational amplifier 62 has a specific offset because of a semiconductor process mismatch, that is, each corresponding output voltage varies even the input voltage is the same for each operational amplifier 62, for example the input voltage is V_1. Thus, DL1, DL2, DL3, ... DLn in the data line 24 have different voltage levels due to above-mentioned offset effect of the operational amplifiers 62. Therefore, different voltage levels are stored in each capacitors 30 corresponding to DL1, DL2, DL3, ... ,DLn of the data lines 24. Then, the switch 64 is switched to conduct the ends E1 and E3 to change current routes. Therefore, the voltage V_1 transmitted by the metal line 66 can not drive the capacitors 30 via the operational amplifier 62 owing to the status change of the switch 64. However, each capacitor 30 is connected to the same metal line 66 due to conducting the ends E1 and E3. Thus, all capacitors 30 are balanced quickly via the metal line 66 so as to have the same voltage level with an averaged offset.

[0024] For example, the switch 64 is switched to connect the ends E1 and E2 at first. If

the voltage V_1 is 5V, the voltages of DL1, DL2, DL3, and DL4 in the data line 24 are driven toward 5V via the output buffers formed by the operational amplifiers 62. However, the voltages of DL1, DL2, DL3, and DL4 of the data line 24 vary differently because the offset related to each operational amplifiers 62 is different. For example, the voltages at DL1, DL2, DL3, and DL4 of the data line 24 are 4.8V, 5.1V, 4.7V and 4.9V respectively. At this time, the switch 64 is switched to connect the ends E1 and E3. Since DL1, DL2, DL3, and DL4 of the data line 24 are electrically connected to the same metal line 66 via the ends E1 and E3, therefore, the voltages of DL1, DL2, DL3, DL4 of the data line 24 will generate an average voltage rapidly. In other words, each voltage of DL1, DL2, DL3, and DL4 of the data line 24, which are originally 4.8V, 5.1V, 4.7V and 4.9V respectively, come to an average voltage via the metal line 66. It is noteworthy that original different offsets are averaged to generate an identical offset for each data line 24 mentioned above, and the input voltage is then affected by the same averaged offset to generate the average voltage at each data line 24. In addition, the pixels positioned in the same row will have the same gray level when the pixels are driven by the same voltage generated by the voltage divider 17.

[0025]

Please refer to Fig.4, which is a schematic diagram of a second operational amplifier circuit 70 according to the present invention. The second operational amplifier circuit 70 has a plurality of operational amplifiers 72, 73, 74, and 75 to function as output buffers, and a plurality of switchs S1, S2 related to the operational amplifiers 72, 73, 74, and 75. Please note that only four operational amplifiers are drawn in Fig.4 for simplicity, and the operational amplifiers 72, 73, 74, and 75 and switches S1, and S2 are used to drive corresponding pixels through data lines DL1, DL2, DL3, and DL4. The operation of the second operational amplifier circuit 70 is described as follows. In the beginning, each switch S1 is first turned on to make the operational amplifiers 72, 73, 74, and 75 electrically connected to corresponding data lines DL1, DL2, DL3, and DL4. As mentioned before, each operational amplifier 72, 73, 74, and 75 has a unique offset respectively affecting the output voltage to deviate from the input voltage. In other words, if the pixels with regard to the operational amplifiers 72, and 73 are prepared to be driven by the same input voltage level, for instance V1, the voltage levels of the data lines DL1, and DL2 are different owing to the respective offsets corresponding to the operational amplifiers 72, and 73. Then,

all the switches S1 related to the operational amplifiers 72, 73, 74, and 75 are turned off simultaneously. Next, if the operational amplifiers 72, and 73 prepare to drive corresponding pixels toward the same gray level through data lines DL1, and DL2, the switch S2 related to the operational amplifiers 72, and 73 is then turned on. Therefore, the voltage levels of the data lines DL1, and DL2 will quickly approach an average voltage from these two voltage levels. That is, the original offsets are averaged to generate the average voltage for the data lines DL1, and DL2. Similarly, if the operational amplifiers 73, and 74 prepare to drive corresponding pixels toward the same gray level through data lines DL2, and DL3, the switch S2 related to the operational amplifiers 73, and 74 is then turned on as well. Therefore, any adjacent pixels driven by the same input voltage will finally have the same gray level with the help of switch S2. To sum up, voltage at each data line DL1, DL2, DL3, or DL4 is first driven by a corresponding operational amplifier 72, 73, 74, or 75 after the switch S1 related to each operational amplifier 72, 73, 74, or 75 is turned on. Then, each switch S1 is turned off. In addition, the switch S2 is turned on when related adjacent pixels related to the switch S2 are prepared to have the same gray level. Finally, the voltage deviation between the adjacent data lines is eliminated by averaging the offsets generated by the corresponding operational amplifiers through the switch S2. In the preferred embodiment, the second operational amplifier circuit 70 is applied on a LCD panel driven according to a line inversion method. Because the pixels positioned in the same row will have the same polarity according to the line inversion method, the switch S2 is capable of averaging voltages with the same polarity at adjacent data lines such as data lines DL1, and DL2. In addition, the different offsets are not averaged through the voltage selection module 56 shown in Fig.3 but are averaged through the related switch S2. Therefore, any voltage divider circuit that can provide the operational amplifier circuit 70 with different voltage levels is suitable for the first driving circuit 16 in the preferred embodiment.

[0026]

Please refer to Fig.5, which is a schematic diagram of a third operational amplifier circuit 80 according to the present invention. The third operational amplifier circuit 80 is similar to the second operational amplifier circuit 70. Only the arrangement of the switches S1, and S2 is different. As shown in Fig.5, there is a switch S2 electrically connected to the operational amplifiers 72, 74, and another switch S2 is electrically

connected to the operational amplifiers 73, 75. That is, the adjacent data lines such as DL1, and DL2 are not connected through the switch S2. When pixels are driven by a dot inversion method, a two dot line inversion method, or a column inversion method, adjacent pixels in the same row are driven by voltages with opposite polarities. That is, pixels connected to lines DL1, DL2, DL3, and DL4 respectively have polarities such as "+""-""+""-" or "-""+""-""+". Therefore, the third operational amplifier circuit 80 uses switches S2 connected to adjacent operational amplifiers that have the same polarity for averaging above-mentioned offsets when corresponding pixels with the same polarity are driven to the identical gray level. For example, if the pixels connected to the data lines DL1, and DL3 are going to have the same gray level, the switches S1 corresponding to operational amplifiers 72, and 74 are first turned on in the beginning. Because the offsets related to the operational amplifiers 72, and 74 are different, the voltages at the data lines DL1, and DL3 are different as well. Then, the switch S2 related to the lines DL1, and DL3 is turned on. Therefore, the voltage deviation between the lines DL1, and DL3 is eliminated by averaging the offsets generated by the corresponding operational amplifiers 72, and 74. It is noteworthy that the offsets generated from the operational amplifiers 72, and 74 are averaged to generate an average voltage at both lines DL1, and DL3. In other words, the lines DL1, and DL3 still have an averaged offset according to the present invention. But, the voltages at data lines DL1, and DL3 are equal after all. In addition, if two adjacent pixels are not going to have the same gray level, the switch S2 related to the corresponding pixels is kept off without affecting the gray levels of the adjacent pixels. In the preferred embodiment, the switch S2 is connected to two data lines driven according to the same polarity, and these two data lines is spaced by another data line driven according to an opposite polarity. That is, the third operational amplifier circuit 80 is applied on an LCD panel driven by a column inversion method, a dot inversion method, or a two dot line inversion. In addition, the different offsets are not averaged through the voltage selection module 56 shown in Fig.3 but are averaged through the related switch S2. Therefore, any voltage divider circuit that can provide the operational amplifier circuit 70 with different voltage levels is suitable for the first driving circuit 16 in the preferred embodiment.

[0027]

Please refer to Fig.6, which is a simplified diagram of a connection between pixels

82 and the third operational amplifier circuit 80 shown in fig.5. A specific color is generated by mixing three monochromatic lights such as a red light, a green light, and a blue light respectively having different intensities. Therefore, pixels 82 located at the same row are individually responsible for providing a gray level with regard to the red light, the green light, or the blue light. As shown in Fig.6, there are pixels 82 used to represent a color sequence "RGBRGBRGBRGB". When the pixels 82 are driven according to a dot inversion method, a two dot line inversion method, or a column inversion method, adjacent pixels 82 will have opposite polarities. For example, the pixels 82 are driven according to a polarity sequence "+-+-+-+-+-+-". Concerning the red light, the pixels 82a and 82c have the same polarity "+", and the pixels 82b and 82d have the same polarity "-". For the pixels 82a, 82b, 82c, and 82d with regard to the red light, one switch S2 is connected between the pixels 82a and 82c driven by the same polarity "+". In addition, another switch S2 is connected between the pixels 82b and 82d. Therefore, when the third operational amplifier circuit 80 is used to drive pixels with regard to one specific monochromatic light, a switch S2 is responsible for equaling voltages inputted into two adjacent pixels driven by the same polarity and driven to the same gray level. It is noteworthy that the above-mentioned driving method is also applied on driving pixels with regard to green light and blue light, and the repeated description is skipped for simplicity.

[0028]

The voltage selection module 56 shown in Fig.3 is used to provide the operational amplifier circuit 60 with appropriate voltage levels. In addition, the metal lines 66 within the voltage selection module 56 not only transmit electric power but also average voltage levels at different data lines 24. That is, the pixels located at different positions in the same row will have the same gray level when driven by the same voltage provided by the voltage selection module 56. The metal line 66 performs a global voltage average operation. The operational amplifier circuits 70, and 80 shown in Fig.4 and Fig.5 use switches S2 to perform the local voltage average operation. That is, the switch S2 is turned on only when two adjacent pixels related to the switch S2 are prepared to be driven by an identical voltage level. Users are only sensitive to gray level difference between adjacent pixels, but are not sensitive to the gray level of each pixel. Therefore, the objective of the operational amplifier circuits 70, and 80 is to eliminate the gray level difference between adjacent pixels when the adjacent pixels

are driven by the same voltage level. That is, switches S2 of the operational amplifier circuits 70, and 80 take place of the metal lines 66 located in the voltage selection module 56 for eliminating voltage deviations between two adjacent pixels only to achieve a uniform gray level.

[0029] As mentioned above, the second operational amplifier circuit 70 is applied on an LCD monitor driven by a line inversion method, and the third operational amplifier circuit 80 is applied on an LCD monitor driven by a column inversion method, a dot inversion method, or a two dot line inversion. Therefore, the operational amplifier circuit according to the present invention can be applied on an LCD monitor, which is driven according to a predetermined method, to solve the offset deviation problem. In addition, the TFT LCD according to the present invention further comprises a XOR logic circuit or a comparator to determine whether the switche S2 is turned on or not. That is, the XOR logic circuit is used to compare digital input driving data related two pixels to check whether the pixels are going to have the same gray level, and the comparator is used to compare analog input driving data related to two pixels to check whether the pixels are going to have the same gray level. When the XOR logic circuit or the comparator acknowledges that two pixels are prepared to be driven toward the same gray level, the switch S2 related to the pixels will be turned on to eliminate the offset deviation. In other words, the TFT LCD has a detecting circuit such as a XOR logic circuit for digital driving data or a comparator for analog driving data to compare driving data with regard to two pixels. When these two pixels are going to have the same gray level, the switch S2 related to these two pixels is turned on according to a comparison result generated from the XOR logic circuit or the comparator. Furthermore, the present invention is capable of using operational transconductance amplifiers instead of the operational amplifiers to drive the pixels.

[0030] The switches 64 shown in Fig.3 and switches S1, S2 shown in Figs.4~6 are controlled by a timing controller of the present invention. That is, the timing controller teams up with the control circuit 14 shown in Fig.1 to drive the LCD panel 12 properly. Please refer to Fig.7, which is a block diagram of a timing controller 90 according to the present invention. The timing controller 90 comprises a frequency divider 92, a counter 94, a comparator 96, and a logic controller 98. Operation of the timing controller 90 is described as follows. The frequency divider 92 will divide

frequency of a clock signal CLK1 inputted into the frequency divider 92 by a divisor N1. The value of the divisor N1 is determined and set by a control signal Pd. For example, the control signal Pd having a corresponding binary data "00", "01", "10", or "11" will set the value of the divisor N as "1", "2", "3", or "4" respectively. If the frequency of the clock signal CLK is f1, an output signal 102, therefore, has a corresponding frequency f2 equal to f1/N1. That is, when the frequency f1 is 108KHz, and the control signal Pd with a corresponding binary data "11" is inputted into the frequency divider 92, the frequency f2 of the output signal 102 will become 27 (108/4) KHz. In other words, the output signal 102 is adjustable based on the clock signal CLK1 with different frequency values and different divisor settings. Then, the output signal 102 is transmitted to the counter 94. The counter 94 is used to count the output signal 102 based on a predetermined count value N2. For example, when a signal triggers the counter 94 for a predetermined number of times, the counter 94 will output predetermined data C0, C1, C2, and C3 to the comparator 96. That is, a different count value N2 corresponds to different data outputted via C0, C1, C2, and C3. For example, when the counter 94 is triggered by the output signal 102 for 216 times, binary data C0, C1, C2, and C3 having values "1","0","1", and "0" respectively are transmitted to the comparator 96. Because the frequency f2 of the output signal 102 is equal to 27KHz as mentioned above, the output signal 102 will trigger the counter 94 about 27K times per second. Therefore, the counter 94 will output "1", "0", "1", and "0" for C0, C1, C2, and C3 after 8 ms. The comparator 96 will compare the values transmitted by C0, C1, C2, and C3 with a comparing value N3 that is determined and set by a control signal Pc. For example, when the control signal Pc with a binary data "10" is inputted into the comparator 96, the comparing value N3 will be set to "1010". When the values transmitted by C0, C1, C2, and C3 match the comparing value N3, the comparator 96 will generate a voltage level transition. For example, before the counter 94 outputs C0, C1, C2, and C3 with values "1", "0", "1", and "0", the comparator 96 originally outputs value "1". After the output signal 102 triggers the counter 94 with the count value N2, the counter 94 outputs C0, C1, C2, and C3 with values "1", "0", "1", and "0". After the comparator 96 detects that the data transmitted by C0, C1, C2, and C3 (1010) is equal to the comparing value N3 (1010), the comparator 96 will generate a transition from "1" to "0". With the help of a control signal EN, the logic controller 98 can select either the output signal 104 outputted

from the comparator 96 or a clock signal CLK2 generated by an external clock generator. As described above, the output signal 104 is generated through the frequency divider 92, the counter 94, and the comparator 96 positioned inside the timing controller 90. However, the output signal 104 such as the clock signal CLK2 shown in Fig.7 could be directly generated by an external clock generator. The clock signal CLK2 has the same waveform as the output signal 104. Thus, the logic controller 98 determines whether the internal output signal 104 or the external clock signal CLK2 is used based on the control signal EN. For example, when the control signal EN has a binary value "1", the internal output signal 104 is chosen. On the contrary, when the control signal EN has a binary value "0", the external clock signal CLK2 is chosen. It is noteworthy that the selection defined by the control signal EN is adjustable. In other words, when the control signal EN has a binary value "0", the internal output signal 104 is chosen. On the contrary, when the control signal EN has a binary value "1", the external clock signal CLK2 is chosen. To sum up, the user can feed the logic controller 98 with the internal output signal 104 or the external clock signal CLK2 for meeting any types of LCD monitors" driving requirements. Either the output signal 104 of the comparator 96 or the external clock signal CLK2 is used by the logic controller 98 to control the switches 64 shown in Fig.3 and the switches S1, S2 shown in Figs.4~6. That is, when the voltage level of the output signal 104 or the external clock signal CLK2 changes from one level to another level, the average operation performed on voltages for driving pixels toward the same gray level as mentioned above is activated.

[0031]

Please refer to Fig.8, which is a timing diagram of the timing controller 90. The first waveform represents the horizontal synchronization signal 32 shown in Fig.1 for determining activation of one gate line 26. Each gate line 26 is triggered by the horizontal synchronization signal 32 to be active for driving the pixels located at the same active gate line 26. At falling edge of the horizontal synchronization signal 32 related to one gate line 26, the corresponding gate line 26, for example, will be activated by the second driving circuit 18, and the first driving circuit 16 starts to drive the pixels located at the gate line 26 toward specific gray levels related to the pixels. Each gate line 26 is driven sequentially and cyclically, that is, one gate line 26 is driven periodically by the horizontal synchronization signal 32. As shown in Fig.8,

one gate line is activated at time T1 for one driving period, and another gate line will be activated at time T2 for its driving period. The interval between time T2 and T1 is a period of the horizontal synchronization signal 32 related to the corresponding gate line 26. The second waveform represents the clock signal CLK1, and the third waveform represents the output signal 102 generated from the frequency divider 92 shown in Fig.7. It is obvious that the frequency of the output signal 102 is half of the frequency of the clock signal CLK1. In other words, the control signal Pd is inputted into the frequency divider 92 to set the divisor N1 as 2. If the count value N1 that is predetermined to be 8 is obtained by the counter 94, the corresponding values C0, C1, C2, and C3 will be outputted to the comparator 96. Therefore, the control signal Pc is also inputted into the comparator 96 to set the comparing value N3 corresponding the values C0, C1, C2, and C3 related to the count value N1. As shown in Fig.8, the fourth waveform represents the output signal 104, and the output signal 104 holds a value "1" before the counter 94 achieves the predetermined count value N2 that is equal to 8. However, when the count value N1 equal to 8 is achieved by the counter 94, the output signal 104 has a transition from "1" to "0" at time T3, and the output signal 104 will keep a value "0" during time T3 to time T2. After the horizontal synchronization signal 32 activates another gate line at time T2, the counter 94 and the comparator 96 are reset to their initial states. That is, the counter 94 recounts the output signal 102, and the comparator 96 outputs the output signal 104 with a corresponding original value "1". The fifth waveform represents driving voltage of one data line. At time T1, the first driving circuit 16 starts driving the pixel from voltage V_1 to a target voltage V_{254} when the pixel is alternatively driven by opposite polarities to reduce well-known flicker problem. Talking about the switches 64 shown in Fig.3, the switches 64 are controlled by the logic controller 98 to connect nodes E1 and E2 according to the output signal 104. That is, when the output signal 104 has a transition from "0" to "1", the logic controller 98 makes the switches 64 connect the nodes E1 and E2. The pixel is driven by the corresponding operational amplifier 62 based on the voltage V_{254}. Therefore, the driving voltage inputted into the pixel will approach voltage V_{254} after time T4. The output signal 104 has a transition from "1" to "0" at time T3, and the logic controller 98 acknowledges this transition at the same time. The logic controller 98 controls the switches 64 to connect the nodes E1 and E3 after time T3. As mentioned before, because the pixels driven by the same driving

voltage V_{254} are connected together through a metal wire corresponding to the voltage V_{254}, the voltages applies on pixels predetermined to be driven to the same voltage level (V_{254}) are averaged toward a voltage (V_2 for example)close to V_{254} after time T5. After time T2, the pixel, however, will be driven to another voltage with opposite polarity compared with the previous driving operation. As described above, the frequency divider 92, the counter 94, and the comparator 96 are used to generate the output signal 104, and the logic controller 98 controls switches 64 shown in fig.3 based on the output signal 104. The duration of the output signal 104 having a value "1" between time T1 to time T3 is adjustable by choosing appropriate divisor N1, count value N2, and comparing value N3. In addition, the operational amplifiers 62 are no longer used to drive pixels in the preferred embodiment. The operating voltages such as bias voltages inputted into the operational amplifiers 62 are cut off during time T3 and time T2 in the preferred embodiment for reducing total power consumption. Because different LCD monitors have specific loadings, that is, one LCD monitor might spend more time on driving pixels than other LCD monitors. The duration from time T1 to time T3 defines a driving period for the operational amplifiers 62. For the LCD monitor with a small loading, the required duration from time T1 to time T3 is shorter. Therefore, the timing controller 90 can be adjusted to have a shorter duration between time T1 and time T3. The operating voltages related to the operational amplifiers 62 is cut off during time T3 and time T2 for saving power. Similarly, for the LCD monitor with a large loading, the required duration from time T1 to time T3 is longer. Therefore, the timing controller 90 can be adjusted to have a longer duration between time T1 and time T3 for the operational amplifiers 62 to drive pixels toward a target voltage successfully. The operating voltages related to the operational amplifiers 62 is cut off during time T3 and time T2 for saving power as well. From the above description, the same timing controller 90 of the present invention can be applied on different LCD monitors with different loadings, and the output signal 104 is adjustable to meet requirement of each LCD monitor for an optimal power saving capacity. The driving sequence of the switches S1 and S2 shown in Figs.4~6 is similar to the switches 62 shown in Fig.3. During time T1 and time T3, the switches S1 are turned on so that the operational amplifiers 72, 73, 74, 75 can drive corresponding pixels. At time T3, the switches S1 are turned off, and the switches S2 each related to two adjacent pixels driven toward the same gray level by

the same driving voltage inputted into the operational amplifiers before time T3 are simultaneously turned on. The voltages inputted into the adjacent pixels are averaged during time T3 to time T2. Similarly, the operational amplifiers 72, 73, 74, 75 are no longer used to drive pixels. In the preferred embodiment, the operating voltages such as bias voltages inputted into the operational amplifiers 72, 73, 74, 75 are cut off for saving power. Moreover, the power applied to the second power supply 22 and/or the voltage divider 17 also can be cut off for saving more power. Besides, the duration from time T1 to T3 is adjustable based on loading of the LCD monitor. With appropriate settings of divisor N1, count value N2, and comparing value N3 for the timing controller 90, the LCD monitor can save optimal power.

[0032]

In contrast to the prior art, the driving method according to the present invention uses a switch to connect the output terminals of the output buffers. Therefore, the power supply generates a target level to drive some pixels located in a row of the LCD panel toward the same target level. There are different offsets between the output levels of the driving units for driving those pixels toward the same target level. When the output terminals of the output buffers are connected together via the switches, the original different output levels of driving units of corresponding pixels are changed towards an average voltage generated from averaging voltages at output terminals of the driving units of the pixel. Although the average voltage may be not exactly equal to the target level, those pixels, which are located in the same row and are predetermined to be driven toward the same target level, are driven to the same level by using the method of the present invention. Thus, the uniformity problem in the prior art caused by level offsets can be solved. In addition, when the voltage averaging operation starts working, the related output buffers such as power amplifiers are not used for driving pixels during the voltage averaging operation. Therefore, the driving method according to the present invention cuts off any operating voltages such as bias voltages inputted into the output buffers for reducing power consumption. Furthermore, the driving method according to the present invention uses a timing controller to determine activation timing of the voltage averaging operation. The activation timing is adjustable by appropriate settings inputted to the timing controller for meeting different loading of LCD monitors. With suitable activation timing setting, the corresponding LCD monitor can have an optimal

power saving capacity.

[0033] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.